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Efficient representation of cross current effects in contributor-based power models

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**See foot notes [FN] for additional information on each slide.*



Motivation

- Cross current (XC) power is the component of dynamic power that occurs when both pull-up and pull-down networks are on at the same time [FN1].
- As we move to smaller technologies, cross current contribution to overall chip power is notably increasing, with ~15% of dynamic power for IBM POWER9 [1].
- Following the industry standard (IEEE 2416), contributor-based modeling enhances power modeling efficiency by using PVT (Process, Voltage, and Temperature) independent modeling [2].
- We present a new approach to model cross current power in a unique way, that is both accurate and efficient, fitting into the contributor modeling paradigm. This a first in the industry, which is used in the tape out of IBM microprocessors.
- The presented techniques also allow for hierarchical separation of cross current power component, for effective management [FN2] of its consumption, in dynamic power dominated high-performance microprocessors [FN3].

Main Idea

Key Idea

- Model cross current as effective switching capacitance (Ceff) using contributor modeling [FN4].
- Capture slew and load sensitivities using circuit simulation only on subset of circuit topologies for use across the library.
- Hierarchical (Gate & Chip level) segregation of these models for cross current specific evaluation and analyses, in slew and load context.

Key Benefits & Differentiation

- No need of characterization or storing data across PVT corners, slew, load ranges (as opposed to .libs).
- Minimal overhead of computing cross current at desired conditions. No expensive interpolation or extrapolation required.
- Existing approaches need newer circuit simulations to separate cross current component which are expensive and time consuming [3].
- Hierarchical separation of cross current power to enable specific analyses towards mitigation and management.

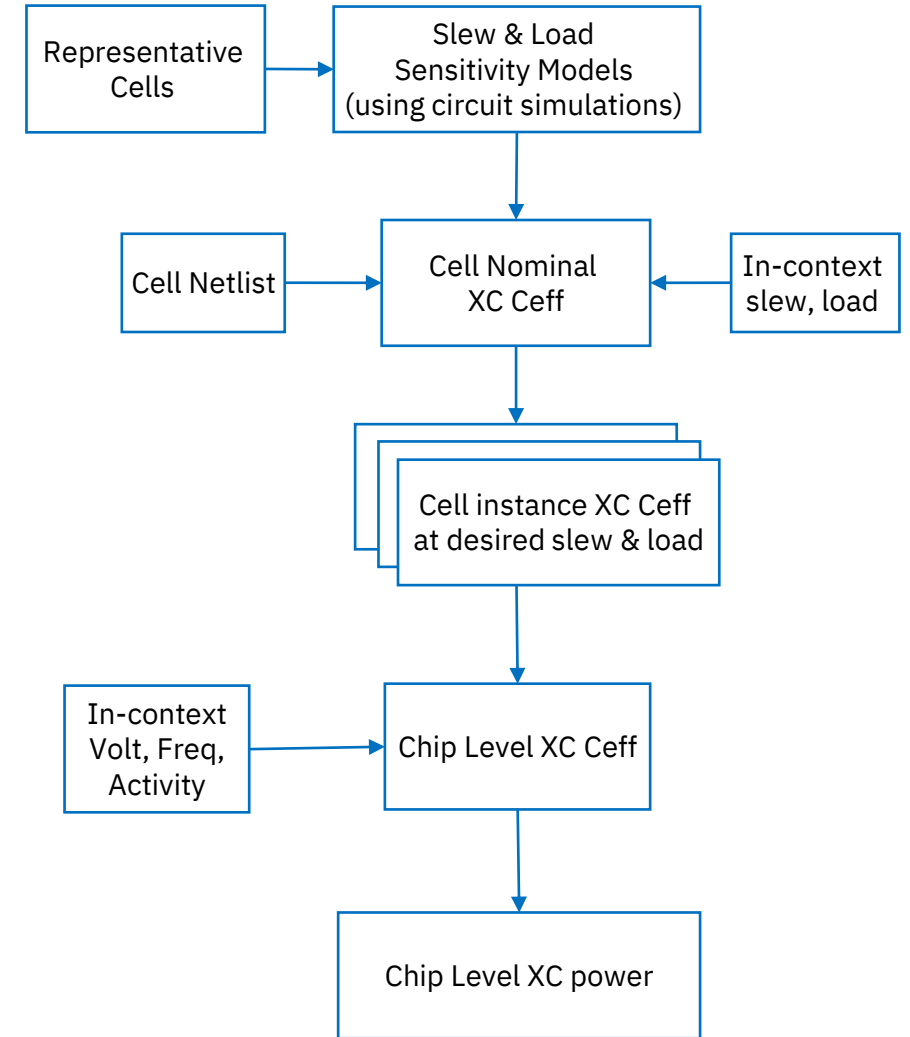


Figure 1. Overall flow for cross current power modeling and computation

Key Idea: Details

- For a given PVT corner, cross current ceff/power can be accurately estimated at any desired input slew and output load (slew-load) condition from the nominal [FN5] value, using slew & load sensitivity models.
- The slew and load sensitivity models are determined by performing circuit simulations on representative circuits chosen empirically [FN6] over a range of slew-load combinations. They are modeled as polynomial functions of cell characteristics, input slew, output load and these sensitivities are applied for modeling the entire library.
- The nominal cross current Ceff is computed out-of-context at the cell/macro level. Using the sensitivity models and in-context slew, load at the higher (macro/chip) level, cross current Ceff at conditions is computed.
- Modeling XC as a Ceff allows for hierarchical tracking of this component at different design levels for specific analyses. We can compute data and clock XC contribution at cell, macro, unit and chip levels at any desired conditions.
- For illustrative purposes, a simplistic form of the models [FN7] can be

$$XC_{slew,load} = \text{Nominal XC} + \text{XC Slew Sensitivity Model} - \text{XC Load Sensitivity Model}$$

$$XC_{slew,load} = \text{Nominal XC} + \text{Drive Strength} * X1M M_{slew} * (\text{slew} - \text{nominal slew}) \\ - (K1_{slew_load} * \text{slew} * \text{slew} + K2_{slew_load} * \text{slew} + K_{slew_load}) * (\text{load} - \text{nominal load})$$

Experimental Results

- Experiments performed on high-performance, FinFET cell libraries comprising of combinatorial cells, latches, local clock buffers.
- Across cell types (cells with high XC like single-in single-out cells), VT types (low, medium, high), varying cell sizes, and different combinations of Input Slew and Output Loads, for 7nm and 5nm technologies.
- Accuracy was established by comparing the XC power (and Total power) computed using CeFF-Sensitivity techniques and power computed from circuit simulation.
- Total power accuracy is within $\sim +5\%$, with less than $\sim 1\%$ increase in size of the model, and efficiency comparable to existing CeFF models.

Cell1								
Input Slew (s)	Output Load (L)	XC power using CeFF-Sensitivity/ XC power using spice				Total power using CeFF-Sensitivity/ Total power using spice		
		VT_Type1	VT_Type2	VT_Type3		VT_Type1	VT_Type2	VT_Type3
s1	L8	1.09	1.03	0.87		1.00	1.00	0.98
s2	L7	1.17	1.16	1.08		1.01	1.02	1.02
s3	L6	1.21	1.16	1.08		1.02	1.03	1.04
s4	L5	1.21	1.13	1.07		1.03	1.04	1.04
s5	L4	1.19	1.10	1.05		1.04	1.05	1.04
s6	L3	1.14	1.08	1.04		1.05	1.04	1.03
s7	L2	1.10	1.05	1.03		1.04	1.04	1.03
s8	L1	1.05	1.03	1.02		1.03	1.02	1.02
s9	L1	1.03	1.14	1.08		1.01	1.05	1.04
s10	L2	1.24	1.19	1.10		1.04	1.07	1.06
s11	L3	1.26	1.17	1.09		1.05	1.06	1.05
s12	L4	1.22	1.13	1.07		1.04	1.05	1.04
s13	L5	1.17	1.10	1.05		1.03	1.04	1.03
s14	L6	1.10	1.07	1.04		1.02	1.03	1.02
s15	L7	1.03	1.04	1.02		1.01	1.02	1.01
s16	L8	0.98	1.02	1.01		1.00	1.01	1.01

Cell2								
Input Slew (s)	Output Load (L)	XC power using CeFF-Sensitivity/ XC power using spice				Total power using CeFF-Sensitivity/ Total power using spice		
		VT_Type1	VT_Type2	VT_Type3		VT_Type1	VT_Type2	VT_Type3
s1	L8	1.03	0.98	0.83		1.00	1.00	0.98
s2	L7	1.15	1.15	1.08		1.01	1.02	1.02
s3	L6	1.21	1.16	1.09		1.02	1.03	1.04
s4	L5	1.21	1.14	1.08		1.03	1.05	1.05
s5	L4	1.19	1.12	1.07		1.04	1.05	1.04
s6	L3	1.16	1.09	1.06		1.05	1.05	1.04
s7	L2	1.11	1.07	1.05		1.05	1.05	1.04
s8	L1	1.07	1.05	1.04		1.04	1.04	1.03
s9	L1	0.99	1.12	1.07		1.00	1.04	1.04
s10	L2	1.22	1.19	1.11		1.04	1.07	1.06
s11	L3	1.25	1.18	1.10		1.04	1.07	1.06
s12	L4	1.23	1.15	1.08		1.04	1.06	1.05
s13	L5	1.18	1.11	1.07		1.03	1.04	1.04
s14	L6	1.12	1.08	1.05		1.02	1.03	1.03
s15	L7	1.03	1.06	1.04		1.01	1.02	1.02
s16	L8	0.98	1.03	1.03		1.00	1.01	1.02

Summary

- Cross current power contribution to overall chip power is significant and requires accurate modeling and efficient management across design hierarchies.
- We introduced new techniques to model cross current power for managing workload-based power of dynamic power dominated high-performance hardware designs.
- The cross current power is modeled as a single Ceff model, used across PVT, capturing various sensitivities, and enables hierarchical segregation of power components.
- The approach enables representation of unique cross current contributors into the IEEE 2416 standard.
- Results from IBM microprocessors demonstrates accuracy of the proposed model to be within ~5% , when compared to detailed circuit simulations, with negligible model size increase.